Decomposition and Analysis of Process Variability Using Constrained Principal Component Analysis

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***Abstract*—Process-induced variability has become a predominant limiter of performance and yield of IC products especially in a deep submicron technology. However, it is difficult to accurately model systematic process variability due to the complicated and interrelated nature of physical mechanisms of variation. In this paper, a simple and practical method is presented to decompose process variability using statistics of the measurements from manufacturing inline test structures without assuming any underlying model for process variation. The decomposition method utilizes a variant of principal component analysis and is able to reveal systematic variation signatures existing on a die-to-die and wafer-to-wafer scale individually. Experimental results show that the most dominant die-to-die variation and wafer-to-wafer variation represent 31% and 25% of the total variance of a large set of manufacturing inline parameters in 65-nm SOI CMOS technology. The process variation in RF circuit performance is also analyzed and shown to contain 66% of process variation obtained with manufacturing inline parameters.**

***Index Terms*—Decomposition, principal component analysis, process variation, statistical modeling, variability.**

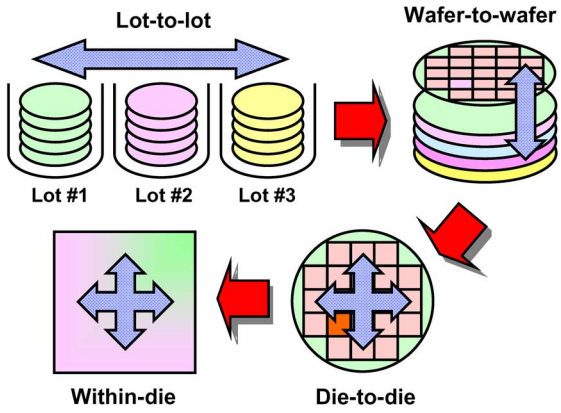

Fig. 1. Definition of four scales of process-induced variability. Lot-to-lot represents process variation in different lots. Wafer-to-wafer process variations exist in different wafers within a lot. Die-to-die means variation in different dies within a wafer. Within-die denotes variation in identical device or circuit within a die.

I. Introduction

PROCESS-INDUCED variation has become a predominant limiter of performance and yield of IC products especially in a deep submicron technology [1]. Variability is introduced from various manufacturing processes such as stress, lithography, deposition, etch, and chemical–mechanical planarization (CMP). However, it becomes increasingly more difficult to accurately model and predict systematic process variability due to the complicated and interrelated nature of physical mechanisms of variation. This paper proposes a statistical method to analyze process-induced variability and separate systematic die-to-die variation and wafer-to-wafer variation [2]. Fig. 1 summarizes the definitions of four different scales of process variation. Lot-to-lot represents process variation existing in different lots. Wafer-to-wafer process variations lie in different wafers within a lot. Die-to-die means variation in different dies within a wafer. Within-die denotes variation in the identical device or circuit within a die. In this paper, two ranges of process variations, namely, die-to-die and wafer-to-wafer variations, are dealt with because of the limitation in the data set available to us.

We exploit measurements from manufacturing inline benchmarking structures (MIBS) that are available in any semiconductor fab for fault detection and device characterization. Using the proposed method and MIBS measurements in the 65-nm SOI CMOS technology, we evaluate the relative amount of systematic die-to-die and wafer-to-wafer variations in the total MIBS measurements. Along with sensitivity analysis of circuit performance to the variation parameters, the contributions of systematic die-to-die and wafer-to-wafer variations can be evaluated separately. Our method also allows us to assess the effect of random variation, which is left as residual and cannot be explained by systematic variation components.

The rest of this paper is organized as follows. Section II explains the notion of MIBS. In Section III, we describe the proposed decomposition method in detail. Experiments of the proposed method are discussed in Section IV. Further applications are introduced in Section V, followed by the conclusion.

II. Manufacturing Inline Benchmarking Structures

MIBS in this paper collectively refer to assorted test structures that are measured in a manufacturing line using a parametric tester for the purpose of defect diagnosis, dc device characterization, and model-to-hardware correlation [3]. For example, FET devices of different sizes and layouts are designed and fabricated for the purpose of regular monitoring

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of critical electrical parameters such as threshold voltage, drive current, and leakage current. Typical MIBS include FETs, ring oscillators, back-end capacitance/resistance test structures, and ground rule validation macros. Wafers in volume production also carry test structures in kerf area to keep track of device/technology characteristics. While a prior work used MIBS data to identify the most correlated device characteristics with respect to circuit performance [4], its full potential has not been explored. In our paper, we exploit a collection of MIBS measurements to find the most representative die-to-die and wafer-to-wafer variations based on the assumption that key device-level parameters such as threshold voltage, gate length, and oxide thickness are embedded in well-chosen MIBS measurements.

III. Decomposition Methodology

In this section, a multivariate statistical analysis technique is presented to separately monitor die-level and wafer-level systematic variations by observing manufacturing inline measurements. Due to the complexity of semiconductor manufacturing processes and environmental factors, die-to-die and wafer-to-wafer variations are more or less intercorrelated. Separation of die-to-die variation and wafer-to-wafer variation makes it easier to conceptualize and analyze a given process variation and its physical mechanism, than otherwise leaving it as a lumped variation.

A. Principal Component Analysis (PCA)

Let us assume that a multivariate signal of interest, $\mathbf{x}$, is a vector of dimension m. The basic idea of PCA is to find the components $y_1, y_2, \ldots, y_n$ so that they explain the maximum amount of variance of $\mathbf{x}$ possible by n linearly transformed components. One usually chooses $n \ll m$ to reduce the dimension of the data. PCA can be intuitively defined using an inductive form. The direction of the first principal component (PC) $\mathbf{w}_1$ is defined by

$$\mathbf{w}_1 = \arg \max_{||\mathbf{w}||=1} E(\mathbf{w}^T \mathbf{x})^2 \tag{1}$$

where $\mathbf{w}_1$ is of the same dimension m as the data vector $\mathbf{x}$. Thus, the first PC is the projection on the direction in which the variance of the projection is maximized. Having determined the first $k-1$ PCs, the kth PC is determined as the PC of the residual

$$\mathbf{w}_k = \arg \max_{||\mathbf{w}||=1} E\left[\mathbf{w}^T \left(\mathbf{x} - \sum_{i=1}^{k-1} \mathbf{w}_i \mathbf{w}_i^T \mathbf{x}\right)\right]^2. \tag{2}$$

The PCs are then given by $y_i = \mathbf{w}_i^T \mathbf{x}$. In practice, computation of the $\mathbf{w}_i$ can be simply accomplished by singular value decomposition (SVD) on the covariance matrix $E[\mathbf{x}\mathbf{x}^T] = \mathbf{C}_{xx}$. If the covariance matrix is not known *a priori*, it is often estimated based on ensemble of data samples. The $\mathbf{w}_i$ is the eigenvector of $\mathbf{C}_{xx}$ that correspond to the n largest eigenvalues of $\mathbf{C}_{xx}$. For convenience, we define an m-by-n matrix $\mathbf{W} = [\mathbf{w}_1|\mathbf{w}_2|\ldots|\mathbf{w}_n]$, thus yielding

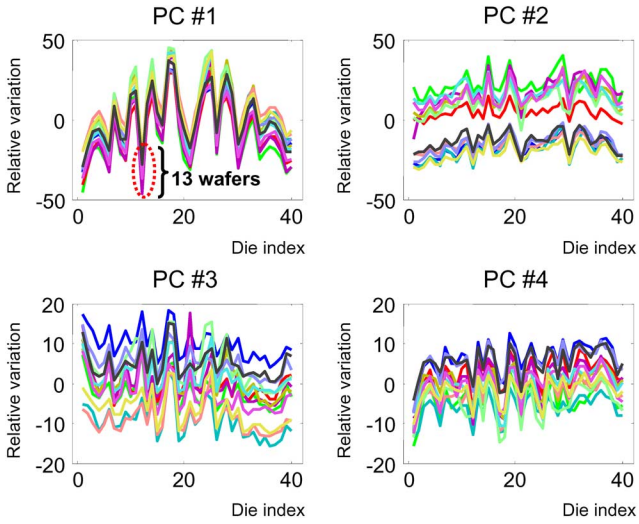

Fig. 2. Four most dominating (ordinary) principal components that contain both wafer-to-wafer and die-to-die variations.

$$\mathbf{y} = \mathbf{W}^T \mathbf{x}. \tag{3}$$

The PCA is a useful multivariate tool to reduce the dimension of data set, to reduce noise, or to visualize the representative features of the given multidimensional data. There has been a growing interest in PCA in the semiconductor manufacturing industry for process failure analysis [5], [6]; however, to the authors' knowledge, there was no previous work to treat die-to-die or wafer-to-wafer variations separately using PCA.

Fig. 2 shows the four most dominating PCs that correspond to the four most representative process variations existing in a large set of inline measurement data from more than 1000 MIBS parameters. Different lines in each graph represent variations for 13 different wafers. It is noted that the first PC contains significantly more die-to-die variation than wafer-to-wafer variation. The second PC has both die-to-die and wafer-to-wafer variations that are comparable in their contributions. Analysis of process variation using ordinary PCA is difficult because the correlated behavior between die-to-die and wafer-to-wafer variations is intractable to understand or model.

B. Constrained Principal Component Analysis (CPCA)

The CPCA is a method to extract constrained PCs (CPCs) which have the same properties as the original PCs but are constrained to a predefined subspace [7]. In our case, only die-to-die and wafer-to-wafer variations are considered. We, thus, have expressions for the most dominant CPC

$$\mathbf{w}_1 = \arg \max_{\mathbf{w} \in \{\mathbf{Q_{d2d}}, \mathbf{Q_{w2w}}\}} E(\mathbf{w}^T \mathbf{x})^2 \tag{4}$$

where $\mathbf{Q_{d2d}}$ and $\mathbf{Q_{w2w}}$ are the orthonormal subspace in die-to-die and wafer-to-wafer directions, respectively. Similar

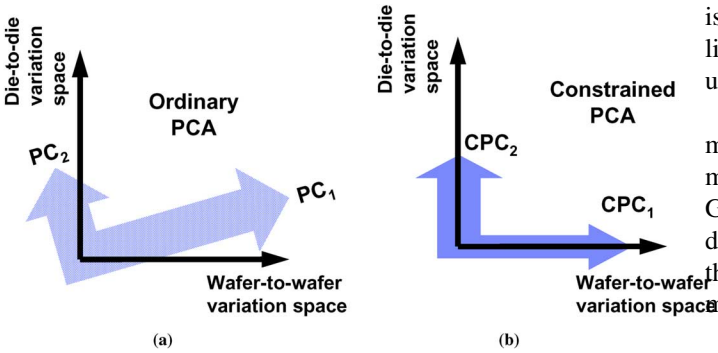

Fig. 3. Comparison of concept of ordinary PC with proposed CPC.

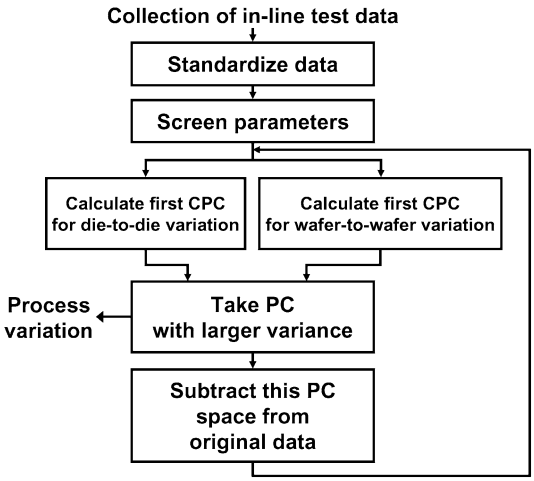

Fig. 4. Flow chart of proposed CPCA algorithm for variability decomposition.

to the ordinary PCA, the CPCA finds CPCs in a sequence of significance. It is useful to extract the PCs of die-to-die or wafer-to-wafer variations separately for a better understanding of the sources of process variations. In the CPCA, PCs can vary only in a guided dimension which is consistent with the die-to-die or wafer-to-wafer variation.

Fig. 3 visualizes the difference between (a) the traditional PCA in the left diagram and (b) the proposed CPCA in the right diagram. Conceptually, the PCA finds orthogonal coordinates which do not generally coincide with die-to-die and wafer-to-wafer variations. Therefore, understanding process variation using the ordinary PCs would be perceptually difficult. On the other hand, the CPCA restricts the PCs to the die and wafer directions, leading to direct visualization of the variation on die-to-die and wafer-to-wafer scales. Only a few CPCs may be examined for this purpose because only a fraction of all the CPCs are sufficient to capture most of the information as with the case of PCs.

C. Decomposition Algorithm

Fig. 4 illustrates how the CPCs can be iteratively obtained. Because the variability of the data is scale-dependent, the PCA is sensitive to the scaling of the data to which it is applied. Thus, at the preprocessing stage, the data set of each MIBS parameter is made zero-mean and unit-variance in order to treat each in-line test parameter insensitive to arbitrary scaling (e.g., different units) and bias (e.g., systematic offset).

Subsequently, all the MIBS parameters which contain meaningless data points (e.g., system default values for failed measurement) are filtered out. In our implementation, a simple Gaussianity test based on kurtosis analysis serves well to detect distributions with significant outliers [8]. Kurtosis (the ratio of the fourth central moment to the square of the variance) is a measure of peakedness of a distribution

$$k(\mathbf{x}) = \frac{E[(\mathbf{x}-\bar{\mathbf{x}})^4]}{(E[(\mathbf{x}-\bar{\mathbf{x}})^2])^2} \tag{5}$$

where $\bar{\mathbf{x}}$ is a mean of $\mathbf{x}$. In our case, the parameters with the kurtosis, greater than eight (having considerably fatter tail than the normal distribution which has kurtosis of three) or less than -2 (having thinner tail than the normal distribution) are flagged unusable. This kurtosis range is generous enough to retain most of single-modal distributions without any outliers.

In the next step, CPCA is performed to calculate the most dominating CPC for die-to-die and wafer-to-wafer variation spaces. Equation (4) is implemented by first averaging original data $(\mathbf{x})$ across all wafers $(\mathbf{x_{d2d}})$ for die-to-die CPC and across all dies $(\mathbf{x_{w2w}})$ for wafer-to-wafer CPC, then finding the first PC on both

$$\mathbf{w_{d2d}} = \arg\max_{||\mathbf{w}||=1} \mathrm{var}\left(\mathbf{w}^T\mathbf{x_{d2d}}\right) \tag{6}$$

$$\mathbf{w_{w2w}} = \arg\max_{||\mathbf{w}||=1} \mathrm{var}\left(\mathbf{w}^T\mathbf{x_{w2w}}\right). \tag{7}$$

These CPCs are calculated in the same way for PCs, by applying SVD to the covariance matrices, $E[\mathbf{x_{d2d}}\mathbf{x_{d2d}}^T]$ and $E[\mathbf{x_{w2w}}\mathbf{x_{w2w}}^T]$. The CPC of larger variance is selected as an output, based on the following test:

$$\mathrm{var}\left(\mathbf{w_{d2d}}^T\mathbf{x_{d2d}}\right) \gtrless \mathrm{var}\left(\mathbf{w_{w2w}}^T\mathbf{x_{w2w}}\right). \tag{8}$$

The data set is, then, transformed to be orthogonal to the space spanned by the selected PC. This routine is iterated for the residual data set until a certain stopping criterion is satisfied.

The resulting PC is constrained to represent either wafer variation or die variation. A CPC representing die-to-die variation may serve as a snapshot of a given lot or technology. Based on this systematic die-to-die pattern, the characteristic of a given lot, or generally a given technology iteration can be monitored, thus allowing fast and pertinent feedback to manufacturing team. Typically, only a few CPCs are sufficient to capture majority of the variation in the whole MIBS parameters, and they are uncorrelated by construction. Therefore, the first few die-to-die variation signatures obtained via CPCA method are likely to reflect physically different process variation sources. For example, the most dominant die-to-die CPC may capture a radial pattern potentially induced by rapid thermal annealing. A CPC for wafer-to-wafer variation in the same lot suggests nonuniformity of process tools used. The correlation study

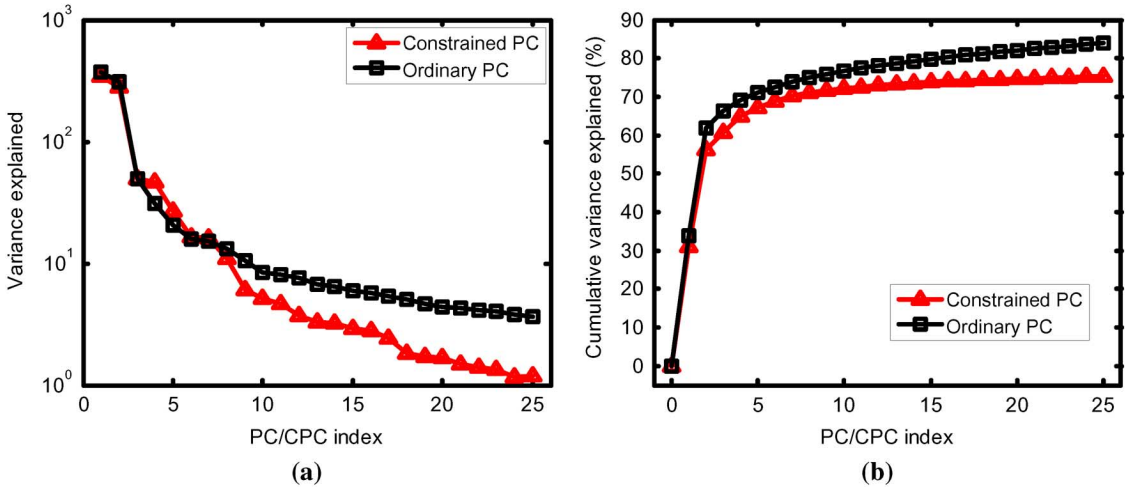

Fig. 5. Variance of first 25 CPCs. Variance of (a) individual and (b) cumulative CPCs are shown.

TABLE I
CATEGORY OF MIBS USED IN THIS EXPERIMENT

MIBS type	Number of parameters before screening	Number of parameters after screening
FET	1988	759
SRAM	398	159
Capacitance	222	108
Ring oscillator	248	83
Total	2856	1109

of die-to-die CPCs with physical process parameters (such as lithography, doping, and CMP) will link how each die-to-die CPC is related to physical processes and remains as future work.

IV. EXPERIMENTS

A. Manufacturing Inline Parameters in 65-nm SOI Technology

For this paper, 1109 parameters from MIBS in a preproduction 65-nm SOI CMOS technology are used. There are 520 samples (40 dies per wafer for 13 wafers) for each inline parameter. The diameter of wafers used is 300 mm, and all 13 wafers are processed in a same lot. There are assorted types of MIBS: FET test structures (e.g., threshold voltage, on and off current), ring oscillators, SRAMs, and capacitance as arranged in Table I. The diverse MIBS measurement data from various test structures ensures that the resulting process variation outputs are representative.

Both ordinary PCA and constrained PCA were performed on the given data set for the purpose of comparison. The computation time was not more than one minute to obtain all the CPCs for this 1109-by-520 inline data matrix. Fig. 5 shows the variance which can be explained by the first 25 PCs and CPCs for the ordinary PCA and CPCA, respectively. A variance for each PC is shown as well as the cumulative variance. The most dominating PC and CPC account for 34% and 31%, respectively, of the total variance of the original data set. Using the first two CPCs, 57% can be explained which is slightly less than 61% for the unconstrained PCs. It is also noted that the CPCs do not reach 100% asymptotically because the die or wafer variation alone cannot fully represent some intertwined relationship between the two. Nonetheless, the advantage of separating the die and wafer components of systematic variation justifies the slightly less coverage of variance by the same number of CPCs compared to the ordinary PCs. In the cumulative variance plot, there is typically a knee region where cumulative variance saturates after a few PC/CPCs. The low-order PC/CPCs beyond saturation correspond to mostly noise components, thus, of little interest for analysis.

Table II lists the type (either die-to-die or wafer-to-wafer) and variance of the first six CPCs. This table also shows that the first and second CPCs capture the die and wafer variation, respectively. The dominant die-to-die variation and wafer-to-wafer variation alternate along the progression of CPCA iteration for the first four CPCs as expected: after one type of variation is subtracted, the other type is likely to be predominant in the residual data at the next CPCA iteration.

Fig. 6 shows the three dominant die-to-die CPC images. They are fitted by the second-order polynomials on the 40 available values for these die-to-die CPCs. The polynomial fitting was done to interpolate the missing values in some chip sites for the purpose of visualization. The first die-to-die CPC shows the slightly off-centered radial pattern. This CPC is the most prominent systematic variation by far, explaining 31% of the variance of the whole data set.

Fig. 7 exhibits the wafer variation captured by the second, fourth, fifth, and sixth CPC corresponding to the first four wafer variations. The second CPC (the most dominating wafer-to-wafer variation) alone represents 25% of the total variance of the whole data set. It is observed that the dominant die variation (31%) is larger than the dominant wafer variation (25%), which is consistent with the recent trend that a die variation is increasingly more important due to the larger wafer size (300 mm) than before, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [9].

TABLE II
TYPE, INDIVIDUAL, AND CUMULATIVE VARIANCE EXPLAINED BY FIRST SEVEN CPCS

CPC index	Type	Variance explained	Cumulative variance explained
1	Die-to-die	31.0%	31.0%
2	Wafer-to-wafer	25.2%	56.2%
3	Die-to-die	4.5%	60.7%
4	Wafer-to-wafer	4.2%	64.9%
5	Wafer-to-wafer	2.4%	67.3%
6	Wafer-to-wafer	1.5%	68.8%
7	Die-to-die	1.4%	70.2%

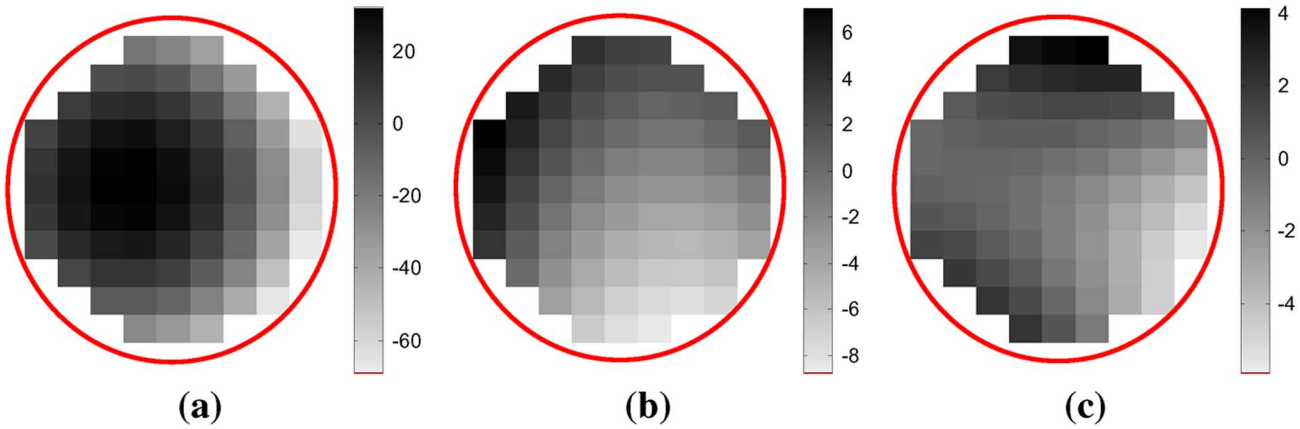

Fig. 6. First three die-to-die CPCs shown as a wafer map. Note that second-order polynomial fitting was performed for these images for purpose of visualization.

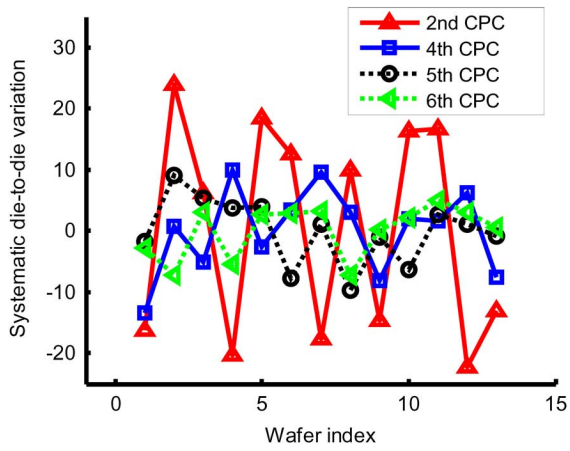

Fig. 7. First four wafer-to-wafer CPCs.

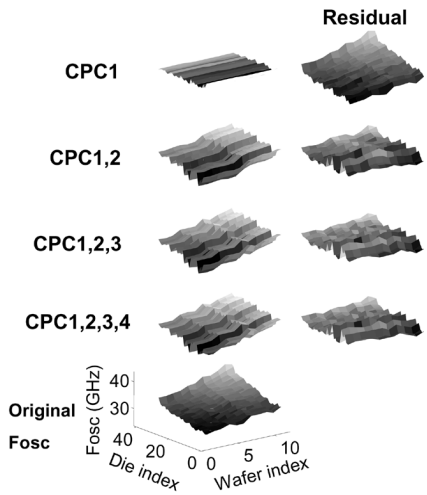

Fig. 8. Self-oscillation frequency of a frequency divider represented by first four CPCs obtained from (left) MIBS measurements and (right) their residuals.

B. Process Variation Analysis on RF Product Performance

CPC decomposition can be applied to a new data set of a totally different nature. For this paper, we used a bench-tested RF self-oscillation frequency (f_{SO}) for a static current-mode logic (CML) frequency divider. A typical phase-locked loop (PLL) block uses a loop structure to lock a free-running voltage-controlled oscillator (VCO) to a desired frequency. A primary frequency divider is one of the key PLL components because it must divide VCO operating frequency into a desired lowered frequency as a high-speed circuit [10]. Measurement of maximum operating frequency (f_{MAX}) is important for yield and performance variation analysis, and it is shown that f_{MAX} closely tracks the divider self-oscillation frequency (f_{SO}) [11]. f_{SO} was measured from the same dies and wafers on which the previous MIBS used for the CPCA reside. Fig. 8 illustrates the sequence of CPCA in three dimensions to visualize how f_{SO} can be reconstructed by adding one component at a time using the first four CPCs.

The bottom left surface shows f_{SO} (z-axis) from different dies and wafers. The top left image is the first CPC, having only die variation. The next image displays the added contribution of the second CPC (wafer variation) on top of the previous image. The images in the right column represent the residuals (original minus reconstructions). This figure demonstrates how original

TABLE III
VARIATION IN RF CIRCUIT PERFORMANCE EXPLAINED BY CPCS OBTAINED WITH MIBS MEASUREMENTS

CPC index	Variance of RF performance (F_{so}) explained by each CPC	Cumulative variance explained
1	5.4%	5.4%
2	36.8%	42.2%
3	21.3%	63.5%
4	2.0%	65.5%

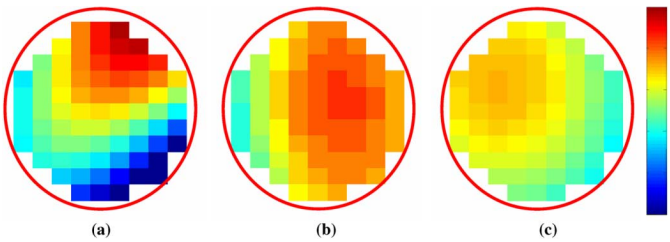

Fig. 9. Dominant die-to-die variation for three evolving 65-nm technology iterations.

data can be successively reconstructed from or, equivalently, decomposed into a few CPCs. Note that these CPCs are calculated from the previous inline dc test data and not from this f_{SO} which is being analyzed. A weight for each CPC is obtained by projecting f_{SO} data on to each CPC space. Table III lists how much variance of RF circuit's performance is explained by each CPC obtained using MIBS measurements. The first four CPCs retain 65.5% of all the information of f_{SO} variation, which is a significant amount especially because the test data (frequency of RF circuit) and the training data for CPC calculation (MIBS measurement data) are quite different in nature. The physical mechanism of how each device-level parameter (MIBS) affects complex RF circuitry such as the frequency divider is beyond the scope of this paper. However, the proposed algorithm and experimental data show that the process variation is substantially systematic, and therefore, the CPCs obtained from MIBS measurements can explain a significant portion of the process variation in complex RF circuits.

V. FURTHER APPLICATIONS

A. Technology Snapshot Monitoring

The most dominating die-to-die variation using CPCA captures the most representative systematic variation on a die-to-die scale and can serve as a snapshot of technology iteration. More than 650 MIBS parameters are used for each 65-nm SOI technology generation. Each MIBS parameter contains 255 samples (15 dies per wafer for 17 wafers). Wafers used are 300 mm and belong to a same lot for a given generation. Fig. 9 shows the dominating die-to-die CPCs for three technology generations, fitted by the second-order polynomials on the 15 available values of the first CPC. The polynomial fitting was done to interpolate the missing values in some chip sites for the purpose of visualization. The run time for CPCA was less than one minute for each generation case. The first generation shows a highly irregular pattern on a wafer scale, presumably from a process anomaly that is common in the first preproduction cycle. In the second and third generations, considerably milder slightly off-centered radial patterns are observed [4].

B. Efficient Sampling for Measurement and Yield Analysis

The most dominant die variation, the first CPC in the previous case in Section IV, contains the most information (31%) about systematic within-wafer variations. Therefore, an intelligent sampling scheme can be proposed for cost-effective measurement and quick yield analysis, based on the first CPC. For example, if only two chips per wafer are allowed for measurement, it would be reasonable to sample the minimum and maximum points in the first die-to-die CPC. One can also selectively measure some sensitive sites to effectively evaluate how much a wafer is compatible to the die variation pattern(s) without sacrificing a great deal of accuracy.

VI. CONCLUSION

In this paper, a statistical method is presented to separate variability components, particularly die-to-die and wafer-to-wafer components, using only measurements from manufacturing inline benchmark structures. The proposed decomposition algorithm is generic and can be easily extended to accommodate other scales of process variation, e.g., within-die or lot-to-lot. A major contribution of the proposed decomposition method is that it allows effective and practical decomposition and visualization of systematic variations using only an ensemble of manufacturing inline electrical data. This analysis can be implemented in a near real time to provide rapid and pertinent feedback to technology development.

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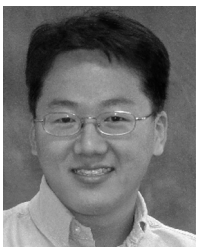

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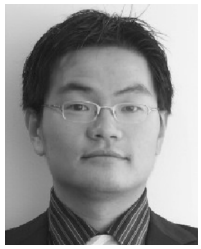
He was with the Samsung Electronics R&D Center at both Giheung, Korea, and San Jose, CA, from 1986 to 1995, where he worked as an RF Engineering Manager to develop transceiver systems for analog and digital cellular phones. He was an RF team leader on many projects, including AMPS, NMT-900, TDMA, and CDMA cellular phones. He was a Research Assistant with the analog design group, University of Minnesota from 1997 to 2001. In 2001, he joined IBM Semiconductor Research and Development Center, East Fishkill, NY. His research interests include RF and low power SOI CMOS integrated circuits and systems, semiconductor passive devices, RF SOC, and CMOS integrated transceivers. He is also working on the 60-GHz transceiver system design by CMOS technology and he has demonstrated many state-of-the-art circuits over 40 GHz based on SOI CMOS technology. He is one of the pioneers for SOI CMOS integrated circuit design over 40 GHz to interact between products and silicon technologies. He is currently working as a Senior Engineer in the performance solution and product-process interaction department at IBM System and Technology Group, East Fishkill, where he is in charge of high-speed and analog benchmark circuits for SOI CMOS technology manufacturing yield. He has authored and coauthored over 50 publications in journals and conferences in the field of RF and high-speed integrated circuits. He also holds or has pending more than 20 U.S. patents.

Dr. Kim received first prize in the 2000 SRC Copper Design Challenge.

Jean-Olivier Plouchart (M'96–SM'06) received the Ph.D. degree in electronics from Paris VI University, France, in 1994.

From 1989 to 1996, he worked with Alcatel, France Telecom, and the University of Michigan on HBT and MESFET MMICs for communication applications. In 1996, he joined the IBM T. J. Watson Research Center as a Research Staff member, where his work involved the design of SiGe BiCMOS and CMOS RFIC circuits for wireless LAN applications, as well as RF product designs for Motorola. In 2000, he lead a team working on low-power high-performance SOI SoC technology and enablement, leading to the first demonstration of 130- and 90-nm SOI ASIC, as well as the enablement of the first 3.5-W 1-GHz Pentium class microprocessor. He also pioneered the design of millimeter-wave SOI CMOS from 30 to 94 GHz in standard microprocessor technology. His research interests include solid-state technologies, the design and optimization of high-speed circuits, the integration of RF transceivers and PLL with microprocessors for SoC applications, the RF measurement automation and the design for yield in nanometer technologies. Currently, he leads the development of nanometer high-speed circuit design and high-yield nanometer design at the IBM T. J. Watson Research Center, Yorktown Heights, NY. He holds two U.S. patents with eight pending and has authored or coauthored over 70 publications.

Dr. Plouchart was a corecipient of the best student paper award from the 2002 IEEE Radio Frequency Integrated Circuit Conference.



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Robert Trzcinski (M'03) joined IBM, Burlington, VT, in 1972, working on the CMOS memory line. In the 1990s, he worked at Poughkeepsie Laser Laboratory, then transferred to Lockheed Martin to work at the Advanced Lithography Facility (ALF) developing an EXCIMER laser steam clean method for X-ray masks, as well as working on the Helios Synchrotron X-ray source and related systems. He returned to IBM to work on direct write E-Beam systems being developed for Nikon. Currently, he is working with the Central Scientific Services team, IBM T. J. Watson Research Center, Yorktown Heights, NY.